**Oscar Alejandro Manzano**

**EE 4513 VLSI**

**Report Lab 7**

**October 16, 2019**

**For this lab, I was able to create a C-switch with no problem by just adding an inverter and then adding the nmos and pmos connecting it appropriated to the diagram and as you can see in the first three pictures, I was able to make it work. After making the C-switch, I created the DFF and that one was a little more challenging because after completing the diagram, and I set up everything I was just getting a 5 v output and after a long debug it was the signal input. C and D were not set correctly. After correcting the problem, I was able to successfully complete the DFF**

**EE 4513 – Fall 2019**

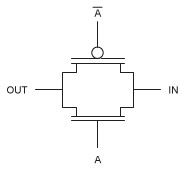
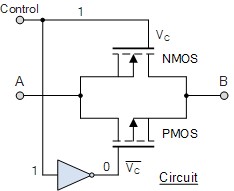
**Lab Assignment #7**

**Objective:**

To learn and implement the layout of simple sequential circuits using standard cells and verify their functionality.

**Tasks:**

1. Draw the layout of a Transmission Gate (Also known as a C – switch) and verify its functionality.



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(a) (b)

Figure 1: (a) Schematic of a Transmission Gate. (b) Typical symbol of transmission gate

1. Using C-switches and inverters create the layout of a positive edge triggered D Flip Flop and verify the functionality. Follow the schematic of a D-Flip Flop given below.

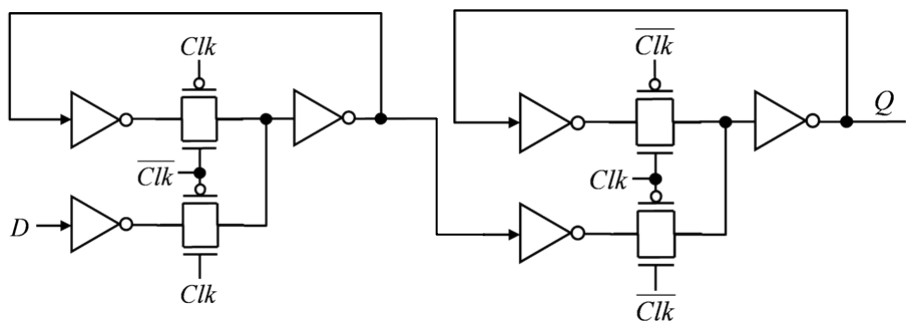
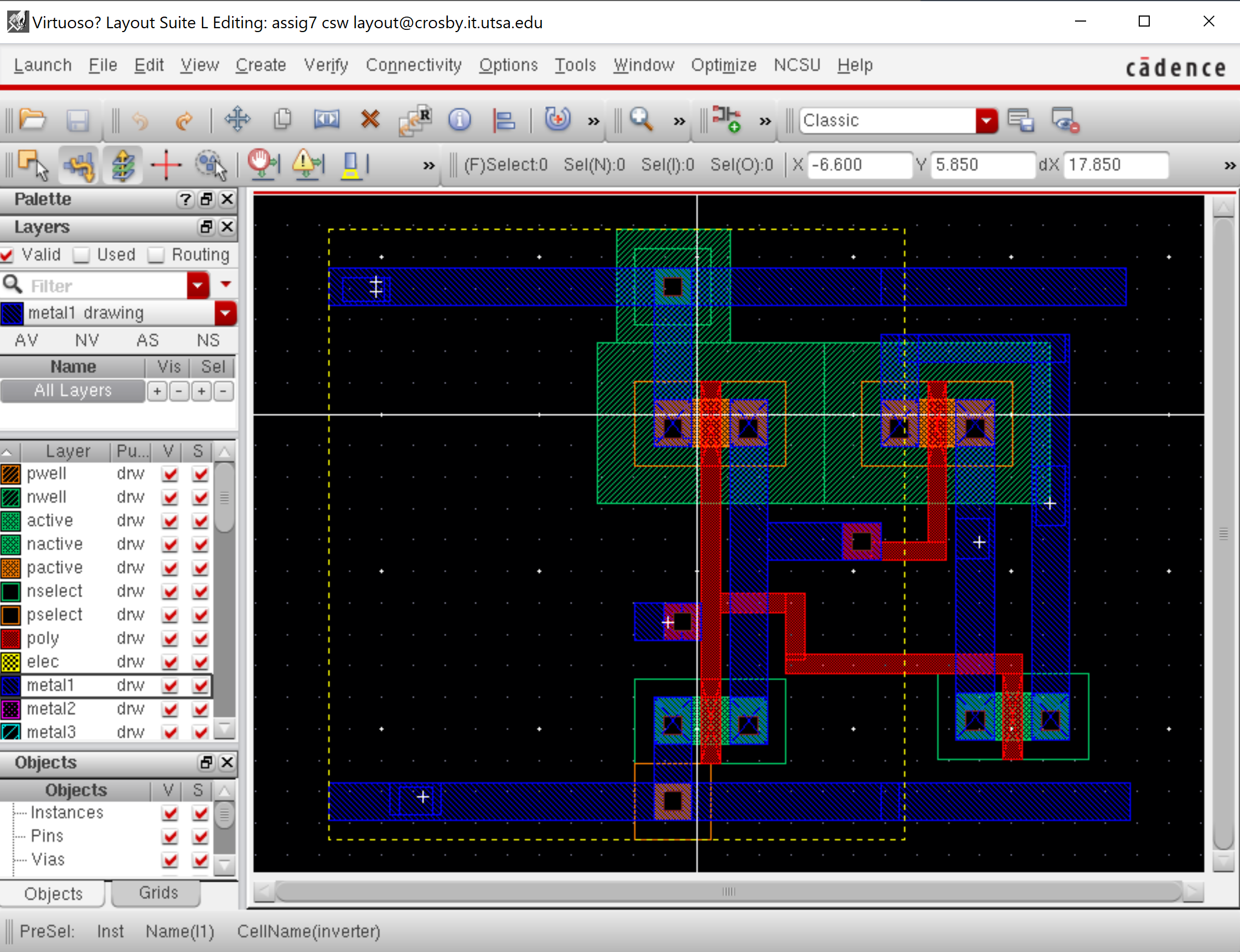


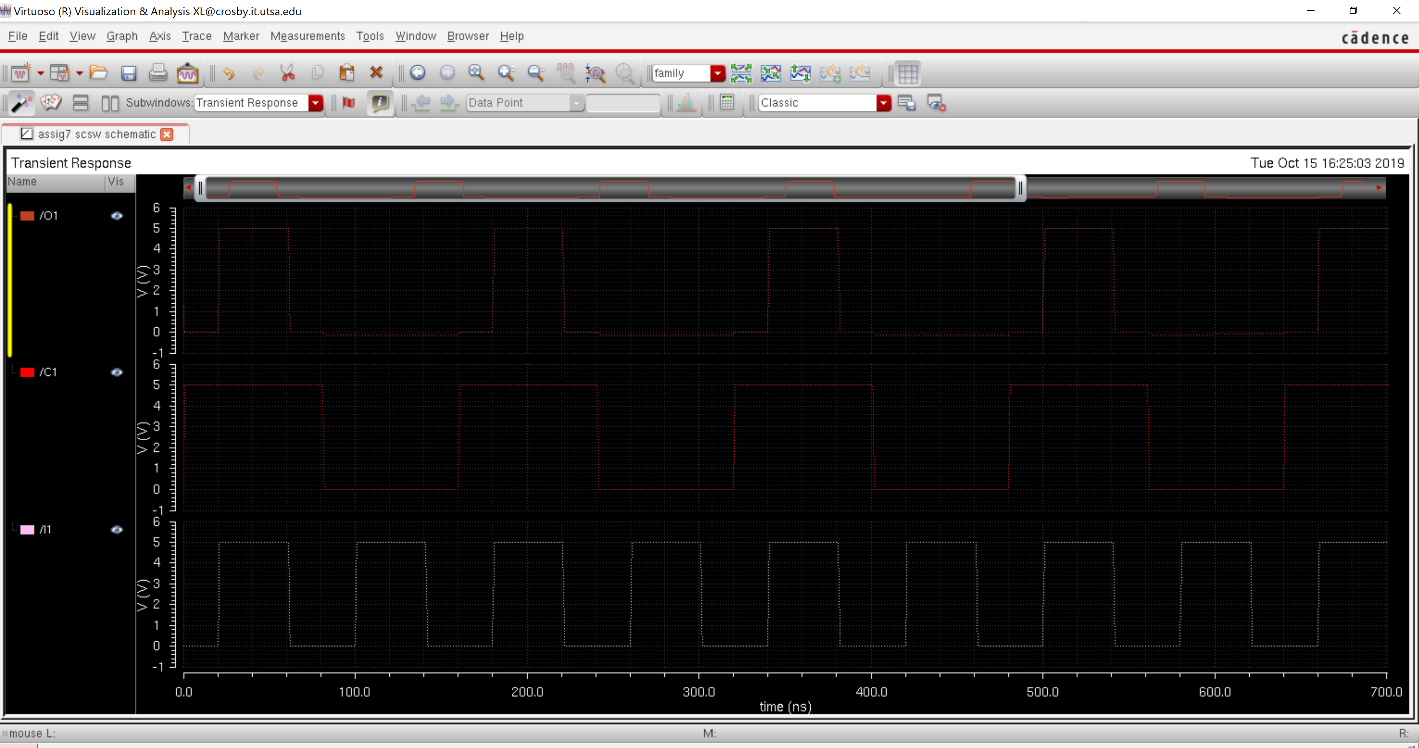
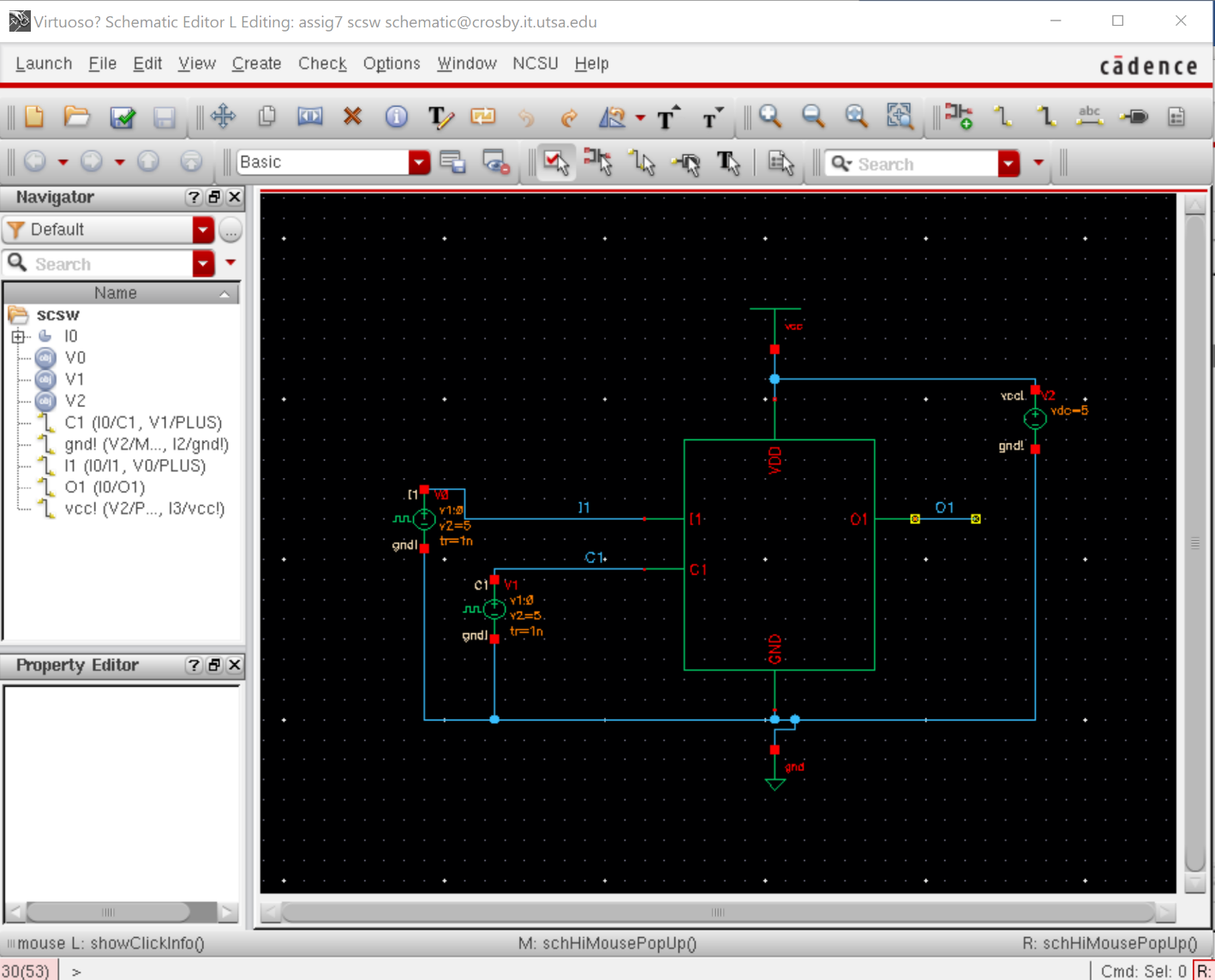
Figure 2: Schematic of A positive edge triggered D Flip Flop using transmission gates and inventers.

**Report:**

You should turn in a report containing the following items:

1. A description of the layout you created, and any challenges faced.
2. Snapshots of layouts and the corresponding simulation waveforms.
3. C-switch





2.DFF

